CHRONTEL

CH7002D

Scalable VGA to NTSC/PAL Encoder

Features

- Fully integrated solution for PC to TV display
- TrueScale ™ rendering engine supports underscan operation for both 640x480 or 800x600 inputs †
- Advanced 3-line digital flicker filtering with programmable algorithm selections †
- Fully programmable through I²C port or hardware (pin-based) controls
- Wide range of VGA software drivers for full synchronization and image positioning
- Auto-detection of TV presence
- Programmable power management features three power-down modes
- Supports both NTSC and PAL (B, D, G, H, or I) TV formats onto both composite and S-Video
- Triple 8-bit ADC inputs and triple 8-bit DAC outputs
- On-chip reference generation and loop filter
- Offered in 44-pin PLCC package

General Description

Chrontel's CH7002 VGA to NTSC/PAL encoder is a stand-alone integrated circuit which provides a PC 99 compliant solution for TV output. It accepts RGB analog inputs directly from VGA controllers and converts them directly into NTSC or PAL TV format, with simultaneous composite and S-Video outputs.

This circuit integrates a digital NTSC/PAL encoder with 8-bit ADC and DAC interfaces, a 3-line vertical filter, and low-jitter phase-locked loop to create outstanding quality video.

Through Chrontel's TrueScale ™ rendering technology, the CH7002 supports full vertical and horizontal underscan operation from either 640x480 or 800x600 input to either NTSC or PAL outputs.

A high level of performance along with full programmability makes the CH7002 ideal for system-level PC or Web browser solutions. All features are software programmable, through a standard I²C port, to enable fully integrated system solutions by using a TV as the primary display device.

† Patent number 5,781,241

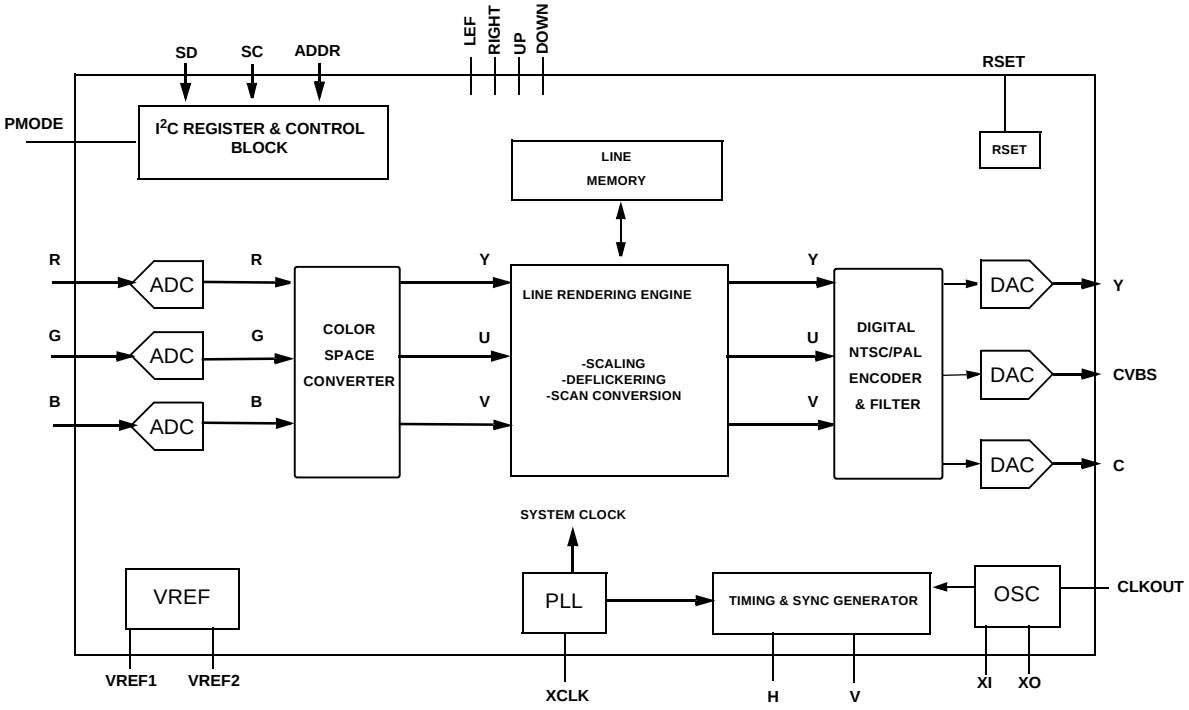


Figure 1: Functional Block Diagram

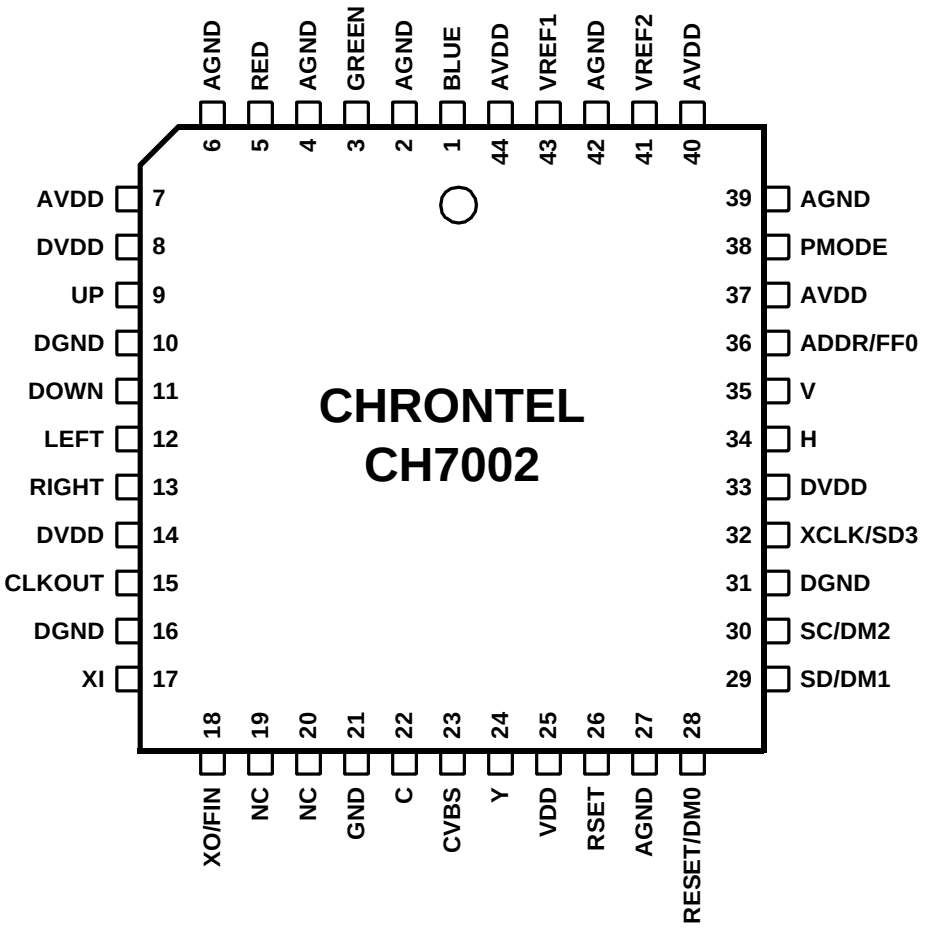


Figure 2: 44-pin PLCC

Table 1. Pin Description

44-Pin PLCC	Type	Symbol	Description
2, 4, 6, 27, 39,42	Power	AGND	**Analog ground** These pins provide the ground reference for the analog section of CH7002, and MUST be connected to the system ground to prevent latchup. Refer to the *Application Information* section for information on proper supply decoupling.
1, 3, 5	In	B, G, R	**VGA Inputs** These pins should be terminated with 75 ohm resistors and isolated from switching digital signals and video output pins. Refer to the *Application Information* section for detailed technical guidance and alternative connection techniques.
7, 37, 40, 44	Power	AVDD	**Analog Supply Voltage** These pins supply the 5V power to the analog section of the CH7002. For information on proper supply decoupling, refer to the *Application Information* section.
15	Out	CLKOUT	**Clock Output** This pin defaults to 14.31818 MHz upon power-up and remains active at all times (including power-down).
8, 14, 33	Power	DVDD	**Digital Supply Voltage** These pins supply the 5V power to the digital section of CH7002. For information on proper supply decoupling, refer to the *Application Information* section.
10, 16, 31	Power	DGND	**Digital Ground** These pins provide the ground reference for the digital section of CH7002, and MUST be connected to the system ground to prevent latchup. For information on proper supply decoupling, refer to the *Application Information* section.
17	In	XI	**Crystal Input** A parallel resonance 14.31818 MHz (± 50 ppm) crystal should be attached between XI and XO/FIN. However, if an external CMOS clock is attached to XO/FIN, XI should be connected to ground.
18	In	XO/FIN	**Crystal Output or External Fref** A 14.31818 MHz (± 50 ppm) crystal may be attached between XO/FIN and XI. An external CMOS compatible clock can be connected to XO/FIN as an alternative.
25	Power	VDD	**DAC Power Supply** These pins supply power to CH7002's internal DACs. Refer to the *Application Information* section for information on proper supply decoupling.
26	In	RSET	**Reference Resistor** A 324 Ω resistor with short and wide traces should be attached between RSET and ground. No other connections should be made to this pin.
21	Power	GND	**DAC Ground** These pins provide the ground reference for CH7002's internal DACs. For information on proper supply decoupling, refer to the *Application Information* section.
24	Out	Y	**Luminance Output** A 75 Ω termination resistor with short traces should be attached between Y and ground for optimum performance. Use of additional filters is discussed in the *Application Information* section.
23	Out	CVBS	**Composite Output** A 75 Ω termination resistor, with short traces, should be attached between CVBS and ground for optimum performance. Use of additional filters is discussed in the *Application Information* section.

Table 1. Pin Description *(continued)*

44-Pin PLCC	Type	Symbol	Description
22	Out	C	**Chrominance Output** A 75 Ω termination resistor, with short traces, should be attached between C and ground for optimum performance. Use of additional filters is discussed in the *Application Information* section.
9, 11, 12, 13	In	UP, DOWN, LEFT, RIGHT	**Position Controls (low-to-high transition, internal pull-up)** UP, DOWN, LEFT, and RIGHT, allows the screen display position to be moved incrementally, in each respective direction, for every toggle of this pin to ground. An internal schmitt trigger minimizes switch bounce problems. These pins may be connected directly to the power supply or ground.
28	In	RESET*/DM0	**Reset (active low) /Display Mode Select [0] (internal pull-up)** The function of this dual use pin is determined by the state of the PMODE pin. When the PMODE pin is kept high (default), the RESET*/DM0 pin becomes RESET*. In this mode, when RESET* is held high (default), the chip is in operating state, and when RESET* is pulled low, the entire chip is reset and initialized to its power-up state. When the PMODE pin is pulled low, this pin becomes DM0, which combined with DM1 and DM2, provides for pin-programming of the 7002 display mode. The pin-programming is "mux-ed" with the Display Mode register selections. All applicable modes are described in *Application Information* and *Registers and Programming* sections.
29	In/Out	SD/DM1	**Serial Data/Display Mode Select [1] (internal pull-up)** The function of this dual use pin is determined by the state of the PMODE pin. When the PMODE pin is kept high (default), this pin becomes SD, the serial data pin of the I^2C interface port. When the PMODE pin is pulled low, this pin becomes DM1, which combined with DM0 and DM2, provides for pin-programming of the 7002 display mode. The pin-programming is "mux-ed" with the Display Mode register selections. All applicable modes are described under the programming section.
30	In	SC/DM2	**Serial Clock/Display Mode Select [2] (internal pull-up)** The function of this dual use pin is determined by the state of the PMODE pin. When the PMODE pin is kept high (default), this pin becomes SC, the serial clock pin of the I^2C interface port. When the PMODE pin is pulled low, this pin becomes DM2, which combined with DM0 and DM1, provides for pin-programming of the 7002 display mode. The pin-programming is "mux-ed" with the Display Mode register selections. All applicable modes are described in the *Registers and Programming* and *Application Information* sections.
32	In	XCLK/SD3	**External Clock/Sample Delay (bit 3) (internal pull-up)** The function of this dual use pin is determined by the state of the PMODE pin. When the PMODE pin is kept high (default), this pin becomes XCLK or external clock, which accepts an external pixel clock input. When the PMODE pin is pulled low, this pin becomes SD3 or Sample Delay, the function corresponding to bit 3 of the Sample Delay register, which provides the following selection: SD3 Sample Delay Selected 1 20 ns nominal delay 0 0 delay (default) This pin-programming is "mux-ed" with the Sample Delay register (bit 3). All related modes are described in the *Registers and Programming* section.
35	In	V	**Vertical Sync Input** This pin accepts the vertical sync output from the VGA card. The capacitive loading on this pin should be kept to a minimum.
34	In	H	**Horizontal Sync Input** This pin accepts the horizontal sync output from the VGA card. The capacitive loading on this pin should be kept to a minimum. Refer to the *Application Information* section for PC Board layout considerations.

Table 1. Pin Description *(continued)*

44-Pin PLCC	Type	Symbol	Description
36	In	ADDR/FF0	**I^2C Address Select/Flicker Filter (bit 0)(internal pull-up)** The function of this dual use pin is determined by the state of the PMODE pin. When the PMODE pin is kept high (default), this pin becomes ADDR or I^2C Address Select, which corresponds to bits **1** and **0** of the I^2C device address (see the *I^2C Control Port Operation* section for details), creating an address selection as follows: ADDR I^2C Address Selected 1 1110101 = 75H = 117 0 1110110 = 76H = 118 When the PMODE pin is pulled low, this pin becomes FF0 or Flicker Filter select, the function of which corresponds to bit 0 of the Flicker Filter register, which selects between the following: FF0 Flicker Filter Mode 0 0:1:0 No filtering 1 1:2:1 Moderate filtering (default) This pin-programming is "mux-ed" with the Flicker Filter register (bit 0). All related modes are described under the *Registers and Programming* section.
38	In	PMODE	**Programming Mode (internal pull-up)** The PMODE pin selects between the two alternative programming modes for the CH7002, which in turn alters the function of five additional pins (RESET/DM0, SD/DM1, SC/DM2, XCLK/SD3, and ADDR/FF0). When PMODE is kept high (default), the chip is placed in I^2C programming mode. When PMODE is pulled low, the chip is placed in direct pin programming mode.
41	In	VREF2	**Internal Voltage Reference** VREF2 provides a typical 2.5V reference that is used as an internal bias to the ADCs. A 0.1 µF decoupling capacitor should be connected between VREF2 and ground.
43	In	VREF1	**ADC Voltage Reference Input / Output** VREF1 provides a typical 1.235V reference that sets the RGB input full scale at 0.75V. A 0.1 µF decoupling capacitor should be connected between VREF1 and ground. VREF1 may also be forced by external reference, where (VFS is the full scale input voltage): VFS ~ VREF1 * 0.75/1.235
19, 20	NC	NC	**No Connect**

Note: For complete information concerning external signal connections, terminations, and system design considerations, refer to the *Application Information* section.

Functional Description

The CH7002 is a fully integrated system solution for converting analog RGB and synchronization signals from a standard VGA source into high-quality NTSC or PAL video signals. This solution involves both hardware and software elements, which work together, to produce an optimum TV screen image based on the original computer generated pixel data. All essential circuitry for this conversion are integrated on chip. On-chip circuitry includes: memory, memory control, scaling, PLL, ADC, DAC, filters, and a NTSC/PAL encoder. All internal signal processing, including NTSC/PAL encoding, is performed using digital techniques, to ensure that the high-quality video signals are not affected by drift issues associated with analog components. No additional adjustment is required during manufacturing.

CH7002 is ideal for stand-alone VGA to NTSC/PAL applications, where a minimum of discrete support components (passive components, parallel resonance 14.31818 MHz crystal) are required for full operation. The CH7002 is designed to provide an ideal solution for computer motherboards, add-on graphics cards, TV-sets, and scan converter boards.

Architectural Overview

The CH7002 is a complete TV output subsystem, using both hardware and software elements, to produce an image on TV, that is virtually identical to the image that would be displayed on a monitor. Creating a compatible TV output from a VGA input is a relatively straightforward process. This process includes a standard conversion from RGB to YUV color space, converting from a non-interlaced to an interlaced frame sequence, then encoding the pixel stream into NTSC or PAL compliant format. However, creating an optimum computer-generated image on a TV screen involves a highly sophisticated process of scaling, deflickering, and filtering. This results in a compatible TV output that displays a sharp and stable image of the right size, with minimal artifacts from the conversion process.

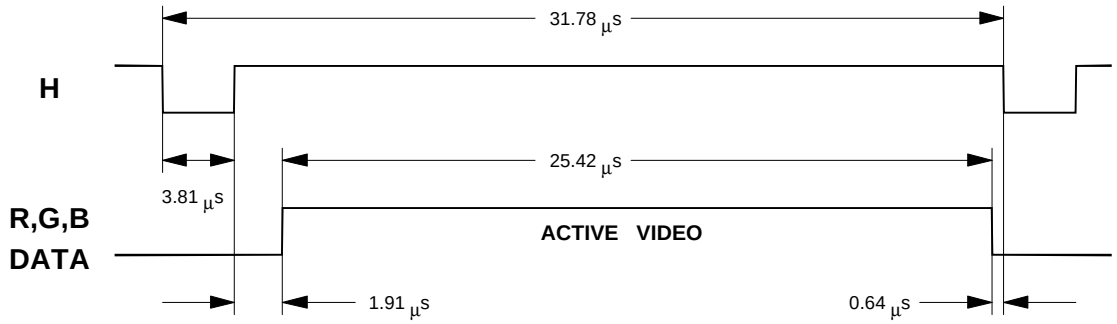
As a key part of the overall system solution, the CH7002 software establishes the correct framework for the VGA input signal to enable this process. Once the display is set to a supported resolution (either 640x480 or 800x600), the CH7002 software may be invoked to establish the appropriate TV output display. The software then programs the various timing parameters of the VGA controller to create an output signal that will be compatible with the chosen resolution, operating mode, and TV format. Adjustments performed in software include pixel clock rates, total pixels per line, and total lines per frame. By performing these adjustments in software, the CH7002 can render a superior TV image, without the added cost of a full frame buffer memory, normally used to implement features such as scaling and full synchronization. Without this added system software, TV output solutions can only guarantee compatible operation in VGA standard mode 12 (640x480x16 color, 60 Hz).

The CH7002 hardware accepts direct VGA outputs (analog RGB inputs), which are digitized on a pixel-by-pixel basis by three 8-bit video A/D converters. The digitized RGB inputs are then color space converted into YUV in 4-2-2 format (encoded into luminance (Y) and color-difference (U,V) signals) and stored in a line buffer memory. The stored pixels are fed into a block where scan-rate conversion, underscan scaling, and 3-line vertical flicker filtering are performed. The scan-rate converter transforms the VGA horizontal scan-rate to either NTSC or PAL scan-rates; the vertical flicker filter eliminates flicker at the output, while the underscan scaling reduces the size of the displayed image to fit onto a TV screen. The resulting YUV signals are filtered through digital filters to minimize aliasing problems. The digital encoder receives the filtered signals and transforms the signals into composite and S-Video outputs, which are converted by the three 8-bit DACs into analog outputs.

Clock Generation and Video Timing

All clock signals of the CH7002 are generated from the VGA synchronization inputs by a low-jitter, PLL circuit. The VGA input and sync timing are illustrated in **Figures 3**, **5 and 6.** The VGA pixel clock is generated internally, using the VGA horizontal sync signal, and is used for sampling the RGB inputs pixel-by-pixel, which aids in preventing aliasing artifacts. All synchronization and color burst envelope pulses are internally generated, using only the timing signals provided by the VGA synchronization inputs.

In situations where the CH7002 is placed next to a graphics controller (e.g. motherboard or add-in cards), the graphics pixel clock can be provided to CH7002, directly from the graphics controller via pin XCLK. This arrangement minimizes phase jitter of the system clock used in the encoder. See the sections on *Application Information* and *Registers and Programming* for detailed information on how to connect and enable this function.



Note: The timing diagram shown is for 640 x 480, 60 Hz VGA mode

Figure 3: Typical VGA Input Timing

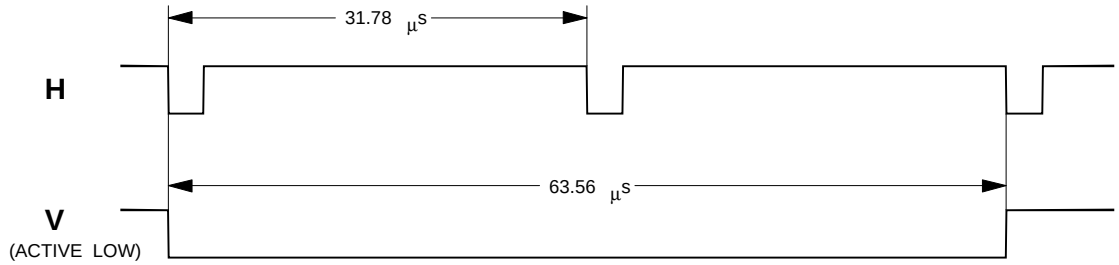


Figure 4: VGA Horizontal and Vertical Sync Input Timing

Note: The values shown in Figures 4 and 5 represent typical timing parameters for VGA controllers operating in 640x480 resolution at 60 Hz, with the CH7002 in overscan mode. Other resolutions and display modes have different timing requirements.

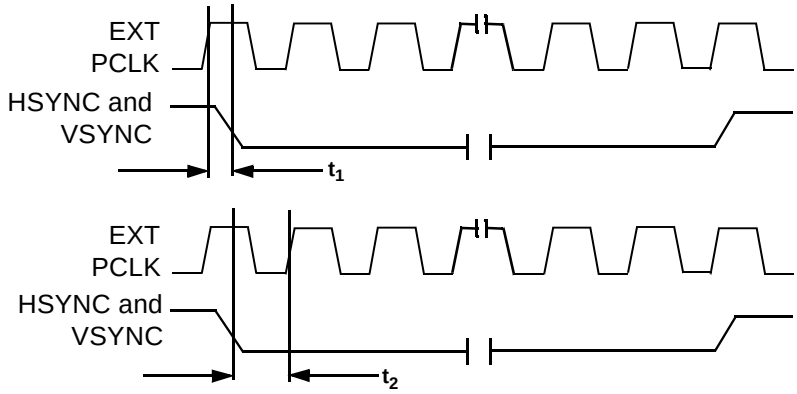


Figure 5: External Clock Input Timing

Color Burst Generation*

The CH7002 employs a proprietary technique for generating the color sub-carrier frequency. This method allows the sub-carrier frequency to be accurately generated from a 14.31818 MHz crystal oscillator, leaving the accuracy of the sub-carrier frequency independent of the sampling rate. As a result, the CH7002 is compatible with any VGA chip, since the CH7002 sub-carrier frequency is not dependent on the pixel rates of VGA manufacturers. This feature is a significant benefit, since even a ± 0.01% sub-carrier frequency variation may be enough to cause some television monitors to lose color lock.

Internal Voltage Reference

The on-chip generated ADC voltage references are brought out to pins VREF1 and VREF2 for decoupling purposes. VREF1 and VREF2 should each have a 0.1 µF decoupling capacitor between each pin and ground. VREF2 provides a typical 2.5V reference used for setting the internal bias to the ADCs. VREF1 provides a typical 1.235V reference used for setting the RGB input full scale at 0.75V. VREF1 can be forced by an external voltage reference to accommodate different RGB input ranges. An additional on-chip bandgap circuit is used, in the DAC, to generate a reference voltage, which in conjunction with a reference resistor at pin RSET, sets the output ranges of the DACs.

For each DAC, the current output per LSB step is determined by the following equation:

ILSB = V(RSET)/RSET * 1/24 = 1.235/324 * 1/24 = 159 uA (nominal)

The value of RSET can be adjusted to achieve a desired output signal level. A valid range for RSET is any value at or over 300 ohms.

Operating Modes

The CH7002 is designed to accept certain limited input resolutions, primarily 640x480 and 800x600, from a VGA type graphics controller. The CH7002 is also designed to support both NTSC and PAL output formats, with scaling to provide either an overscanned or underscanned image, when displayed on a TV. This combination of input resolution and output formatting results in a matrix of operating modes which are listed below, and are described in detail in Table 2. Note that all of these modes may be set either by I^2C programming or by direct pin programming:

- Modes 2 and 3 support 640x480 into a NTSC format in overscan and underscan forms respectively.
- Modes 1 and 4 support 640x480 into a PAL format in underscan and overscan forms respectively. Note that Mode 1 is the recommended operating mode for this resolution because it provides a higher overall quality image.
- Modes 0 and 5 support 800x600 into a PAL format in underscan and overscan forms respectively.
- Mode 6 supports 800x600 into a NTSC format in an underscan form.

Operating Modes *(Continued)*

Table 2. CH7002 Operating Modes

Name	PAL OUT 800x600 IN	PAL OUT 640x480 IN Underscan	NTSC 640x480 IN Overscan	NTSC OUT 640x480 IN Underscan	PAL OUT 640x480 IN Overscan	PAL OUT 800x600 IN Overscan	NTSC OUT 800x600 IN Underscan
Mode	0	1	2	3	4	5	6
Pixel Clock	35.400	25.000	25.175	28.196	25.000	29.500	43.636
Scale Factor	5/6	1/1	1/1	7/8	1/1	1/1	3/4
Total VGA Lines	750	625	525	600	625	625	700
Active VGA Lines	600	480	480	480	480	600	600
Fvert VGA (Hz)	50.0	50.00	59.94	59.94	50.00	50.00	59.94
Fhor VGA (KHz)	37.5	31.250	31.469	35.964	31.250	31.250	41.958
Total TV Lines	625	625	525	525	625	625	525
Active TV Lines	500	480	480	420	480	600	450
Fvert TV (Hz)	50.00	50.00	59.94	59.94	50.00	50.00	59.94
Fhor TV (Hz)	15625.0	15625.0	15734.3	15734.3	15625.0	15625.0	15734.3

Overscan/Underscan

The inclusion of both overscan and underscan forms of output display have been created to enable optimal use of the CH7002 for different application needs. In general, underscan provides an image that is entirely viewable on screen. It should be used as the default for most applications (e.g. viewing text screens, operating games, running productivity applications, working within Windows). Overscan provides an image that bleeds past the edges of the TV screen, exactly like normal television programs and movies appear on TV. It is only recommended for viewing movies or video clips coming from the computer.

Anti-Flicker Filter

The CH7002 integrates a 3-line vertical filter circuit to help eliminate the flicker associated with interlaced displays. When operating in underscan mode, this flicker circuit provides a adaptive filter algorithm for implementing flicker reduction based on an approximate 1:2:1 weighting sequence. When operating in overscan mode, it provides four anti-flicker filter modes as shown in Table 3. These modes are fully selectable, via I^2C, and a subset is selectable (either 0:1:0 filtering or 1:2:1 filtering) when using direct pin programming mode.

Table 3. Anti-Flicker Filter Modes

FF0	FF1	Filter Modes
0	0	0:1:0 averaging (no filtering)
0	1	1:3:1 averaging
1	0	1:2:1 averaging
1	1	1:1:1 averaging

Power Management

The CH7002 supports four operating states (including Normal [On], Power Down, S-Video Off, and Composite Off) to provide optimal power consumption for the application involved. Using the programmable power down modes accessed over the I²C port, the CH7002 may be placed in either Normal state, or any of the four power managed states listed below (see the *Miscellaneous Control Register* under the *Registers and Programming* section). To support power management, a TV sensing function (see *Connection Detect Register*) is provided, which identifies whether a TV is connected to S-Video or Composite, or neither. This sensing function can then be used to enter into the appropriate operating state (e.g., if TV is sensed only on Composite, the S-Video Off mode could be set by software).

Power State	Functional Description
Normal (On):I	In the normal operating state, all functions and pins are active
Power Down:I	In the complete power-down state, most pins and circuitry are disabled.The CLKOUT pin, however, will continue to provide 14.318 Mhz out. This places the CH7002 in its lowest power consumption mode
Composite Off	In Composite-off state, power is shut off to the unused DAC associated with CVBS output, thereby reducing power by approximately 10%
S-Video Off	Power is shut off to the unused DAC associated with CVBS output

When using direct pin-programming mode for the CH7002, only Normal and Power Down states are supported as selected by the Display Mode inputs. When inputs DM[2:0] are set to a 111 state, the CH7002 is placed in Power Down state. The CH7002 operates in Normal mode when the Display Mode settings are set to any valid state (where DM[2:0] is between 000 and 110).

Luminance Filter Options

The CH7002 contains a set of luminance filters to provide a controllable bandwidth output on both composite and S-Video outputs. The response of the luminance filters are shown in the graphs in Figures 7 and 8. The horizontal axis is frequency in Mhz, and the vertical axis is gain in dBs.

The possible S-Video MHz responses are:

Y_SV0: A high frequency response, selected by setting YC-HI to 1 in the Y-filter register.

Y_SV1: A lower frequency response, selected by setting YC-HI to 0 in the Y-filter register.

Y_SV2: A lower frequency response, with peaking enabled, which gives improved transient response, with matching pre-shoot and overshoot of 6%. This is selected by setting YC-HI to 0 and YPEAKD to 0 in the Y-filter register. Note that peaking can only be enabled in the lower frequency response mode.

The possible CVBS (composite) responses are:

Y_CV0: A high frequency response, selected by setting YCV-HI to 1 in the Y-filter register.

Y_CV1: A lower frequency response, selected by setting YCV-HI to 0 in the Y-filter register. This setting will result in a reduced amount of cross-luminance artifacts.

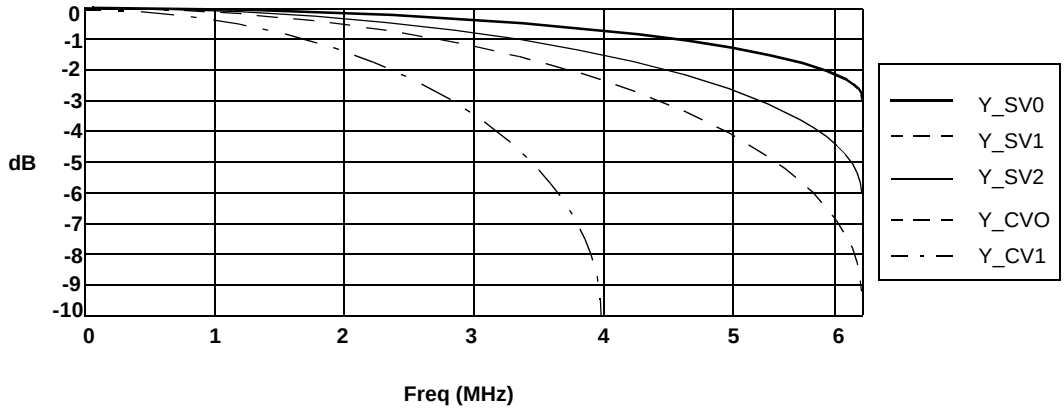


Figure 6: Luminance Frequency Response - Detailed View

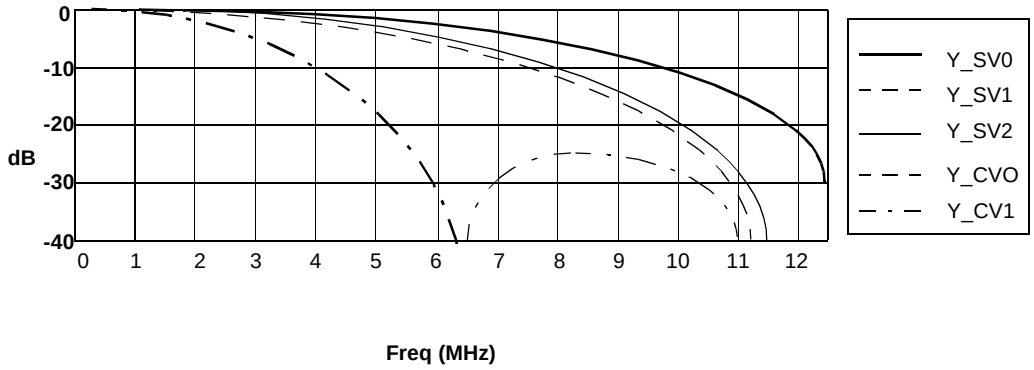


Figure 7: Luminance Frequency Response - Full View

Notes:

1 The curves shown are valid for operating modes 2 and 6. Mode 0 frequency values are 20% higher, mode 1 and 3 frequency values are 12% higher, and mode 4 frequency values are 1% lower, due to changes in clock frequencies.

2 The Y_SV1 and Y_CV0 responses are identical; therefore the curves lie on top of each other.

NTSC and PAL Operation

Composite and S-Video outputs are supported in either NTSC or PAL format. The general parameters used to characterize these outputs are listed in Table 4 and shown in **Figure 8**. (See **Figures 9** through **16** for illustrations of composite and S-Video output waveforms.)

Table 4. NTSC/PAL Composite Output Timing Parameters (in μS)

Symbol	Description	Level (mV)		Duration (uS)	
		NTSC	PAL	NTSC	PAL
A	Front Porch	310	310	1.49 - 1.52	1.50 - 1.78
B	Horizontal Sync	24	24	4.69 - 4.72	4.43 - 4.73
C	Breezeway	310	310	0.60	0.57 - 0.60
D	Color Burst	310	310	2.48 - 2.50	2.33 - 2.52
E	Back Porch	310	310	1.60	1.50 - 1.60
F	Black	363	310	0.92 - 3.64	0.00 - 4.24
G	Active Video	363-1030	310-977	45.40 - 50.84	45.20 - 53.00
H	Black	363	310	0.92 - 3.64	0.00 - 4.24

Notes: For this table and all subsequent figures: RSET = 324 ohms; V(RSET) = 1.235 V; 75 ohms doubly terminated load (BLR=61 for NTSC, and BLR=52 for PAL), 100% amplitude, 100% saturation bars are shown (100%=0.66071V).

1 Durations vary slightly in different modes due to the different clock frequencies used.

2 Active video times vary greatly due to different scaling ratios used in different modes.

3 Black times (F and H) vary with position controls.

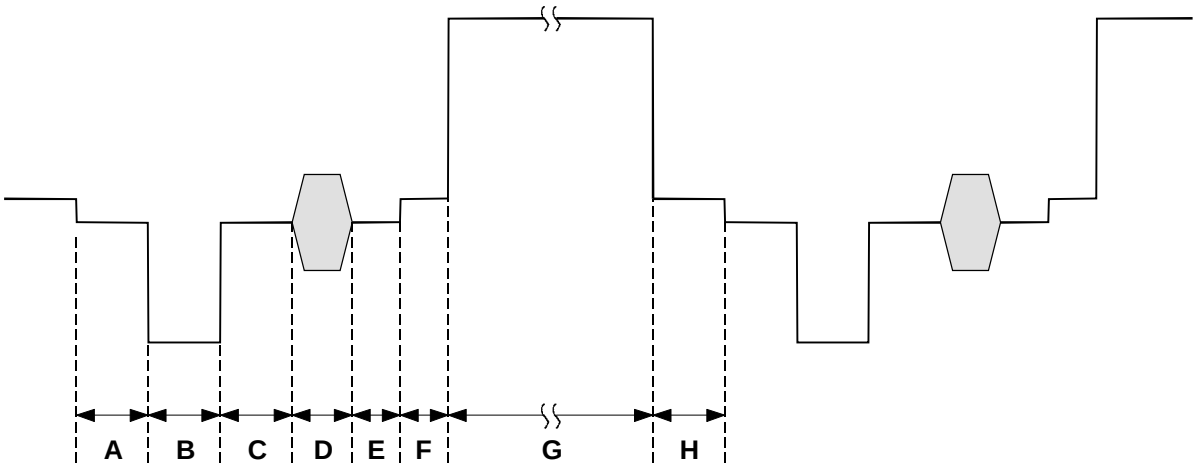
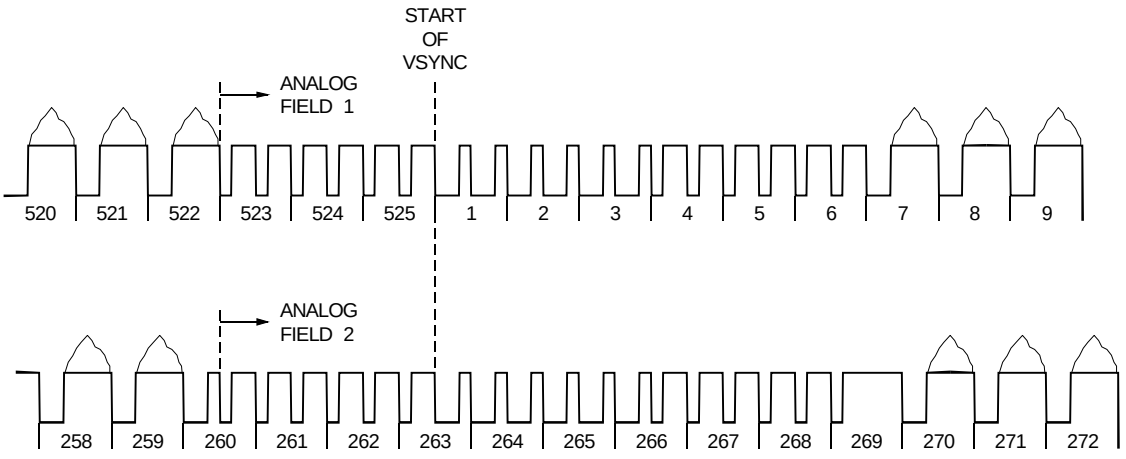


Figure 8: NTSC / PAL Composite Output



LINE RATE = HALF THE VGA LINE RATE IN MODES 1, 2, 4 AND 5

FIELD RATE = VGA VERTICAL REFRESH RATE IN ALL MODES

Figure 9: Interlaced NTSC Video Timing

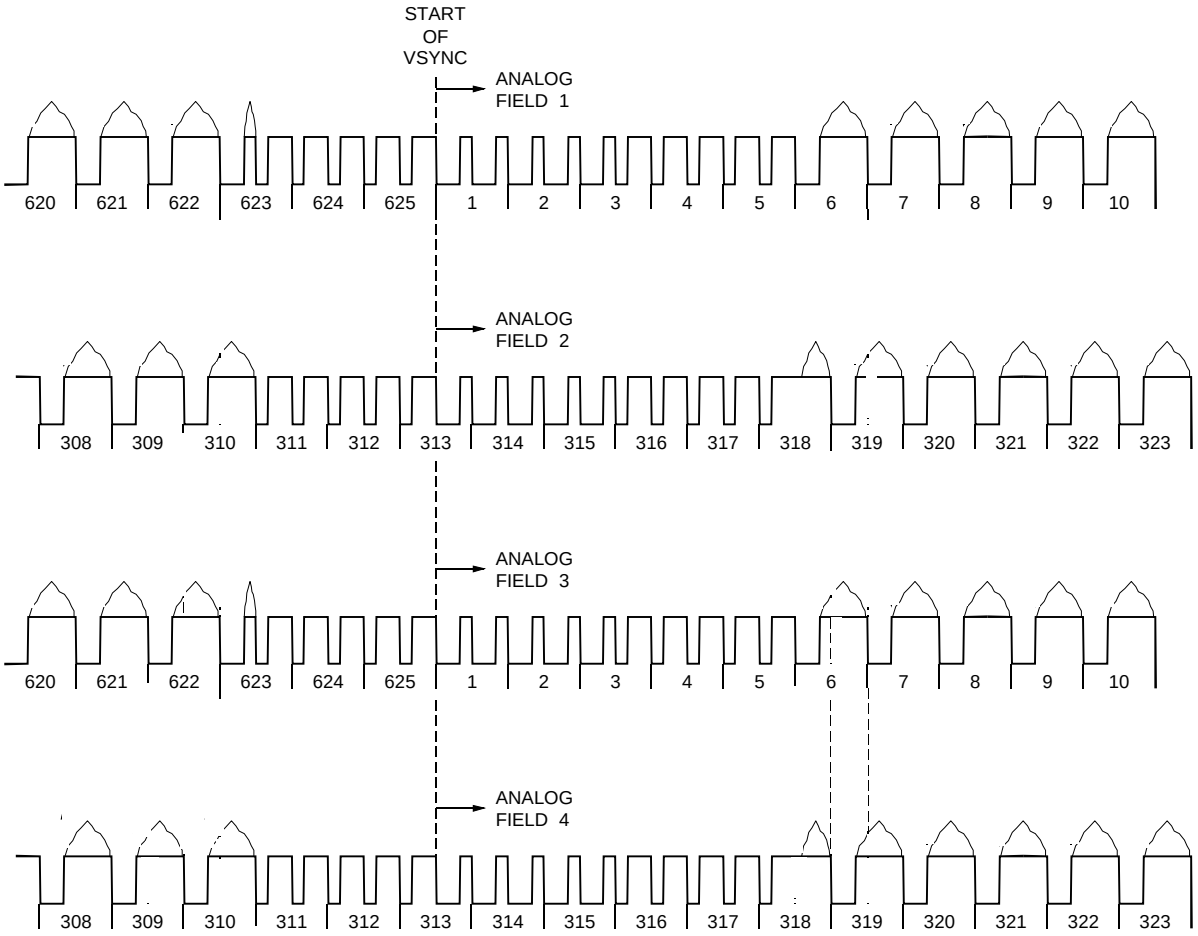


Figure 10: Interlaced PAL Video Timing

Color/Level	mA	V
White	27.48	1.030
Yellow	25.41	0.953
Cyan	22.08	0.828
Green	20.01	0.750
Magenta	16.99	0.637
Red	14.93	0.560
Blue	11.59	0.435
Black	9.69	0.363
Blank	8.26	0.310
Sync	0.64	0024

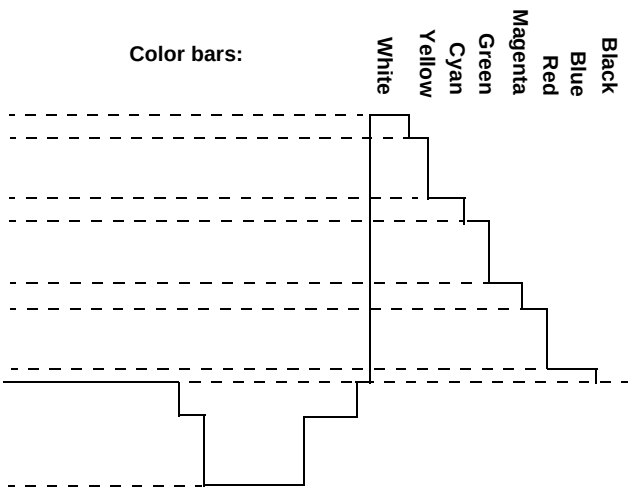


Figure 11: NTSC Y (Luminance) Output Waveform

Color/Level	mA	V
White	26.05	0.977
Yellow	23.98	0.899
Cyan	20.65	0.774
Green	18.58	0.697
Magenta	15.56	0.584
Red	13.50	0.506
Blue	10.16	0.381
Blank	8.26	0.310
Sync	0.64	0.024

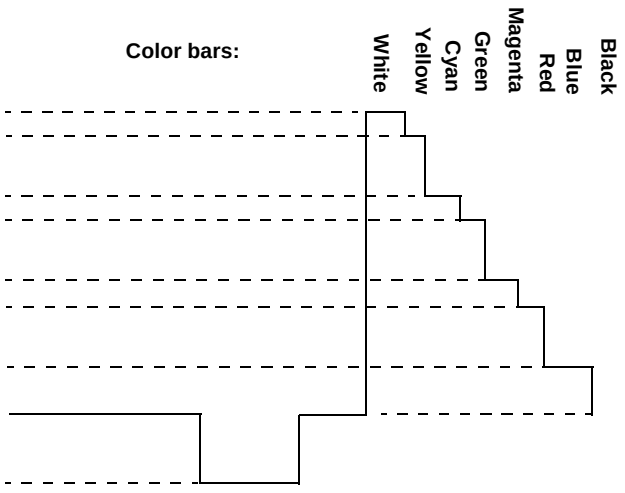


Figure 12: PAL Y (Luminance) Video Output Waveform

Color/Level	mA	V
Cyan/Red	27.00	1.012
Green/Magenta	26.36	0.989
Yellow/Blue	23.82	0.893
Peak Burst	19.69	0.739
Blank	15.88	0.596
Peak Burst	12.07	0.337
Yellow/Blue	7.94	0.298
Green/Magenta	5.40	0.202
Cyan/Red	4.76	0.179

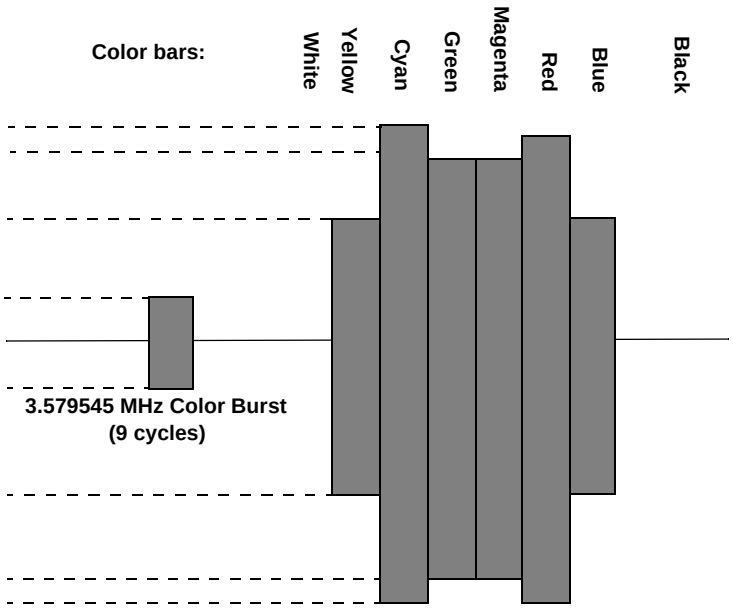


Figure 13: NTSC C (Chrominance) Video Output Waveform

Color/Level	mA	V
Cyan/Red	27.00	1.012
Green/Magenta	26.36	0.989
Yellow/Blue	23.82	0.893
Peak Burst	19.69	0.739
Blank	15.88	0.596
Peak Burst	12.07	0.337
Yellow/Blue	7.94	0.298
Green/Magenta	5.40	0.202
Cyan/Red	4.76	0.179

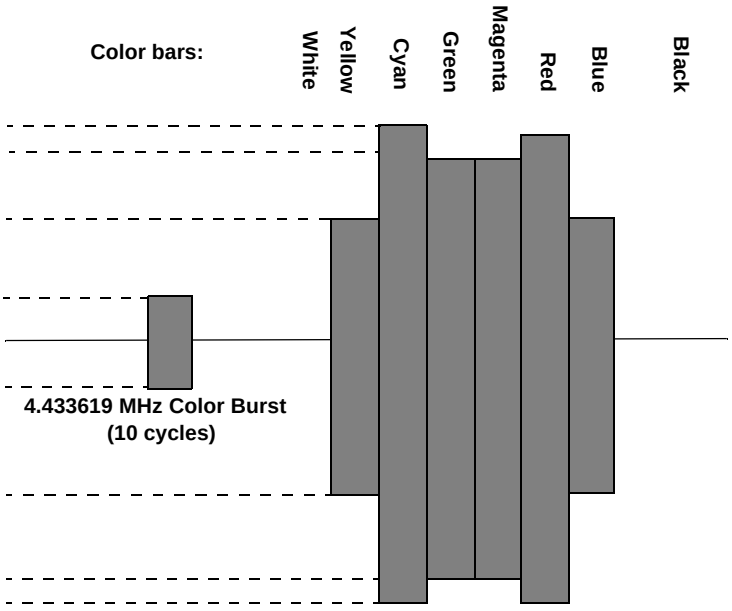


Figure 14: PAL C (Chrominance) Video Output Waveform

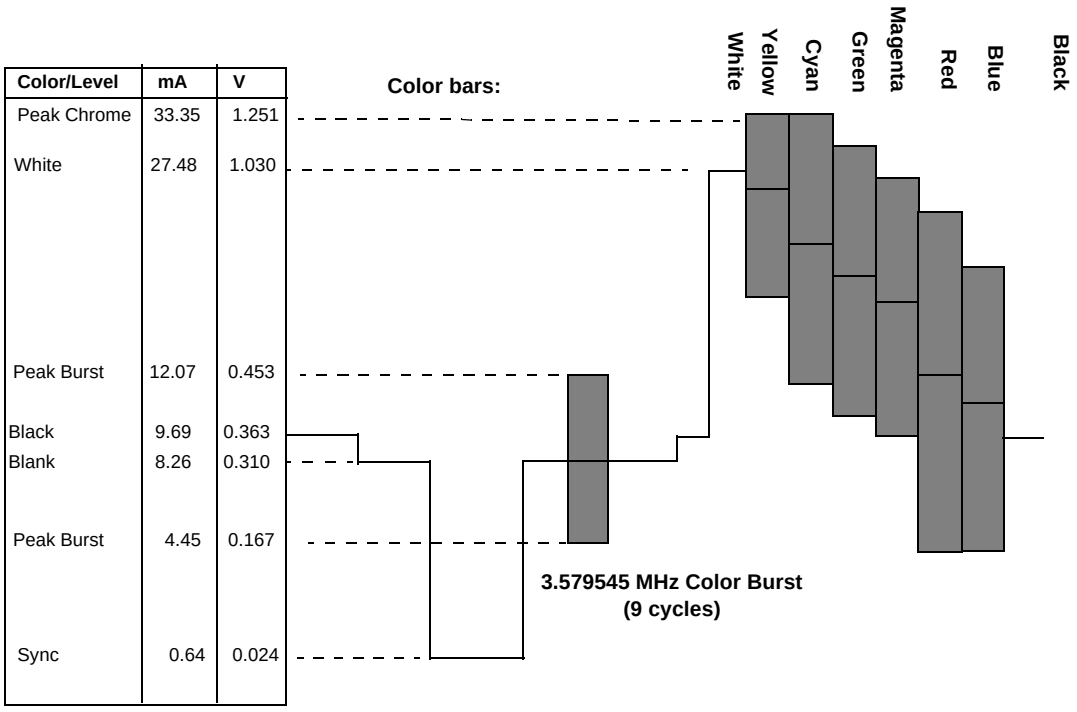


Figure 15: Composite NTSC Video Output Waveform

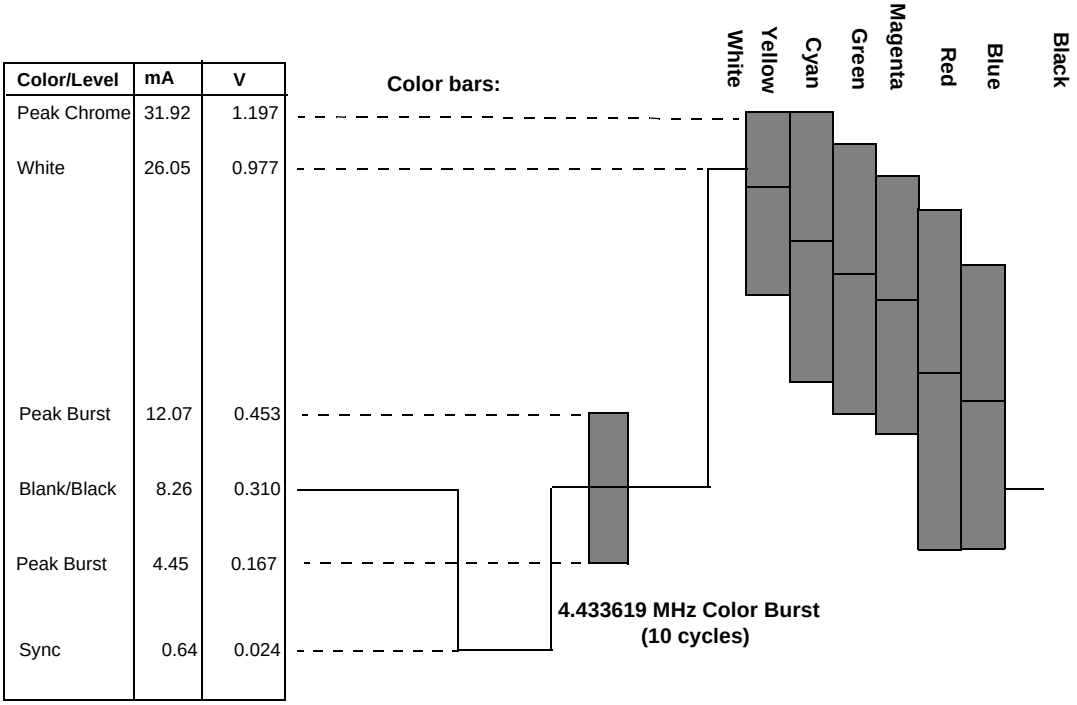


Figure 16: Composite PAL Video Output Waveform

I²C Port Operation

The CH7002 contains a standard I²C control port, through which the control registers can be written and read. This port is comprised of a two-wire serial interface, pins SD (bi-directional) and SC, which can be connected directly to the SDB and SCB buses as shown in **Figure 17**.

The Serial Clock line (SC) is input only and is driven by the output buffer of the master device (also shown in Figure 17). The CH7002 acts as a slave, and generation of clock signals on the bus is always the responsibility of the master device. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the bus can be transferred up to 400 kbit/s.

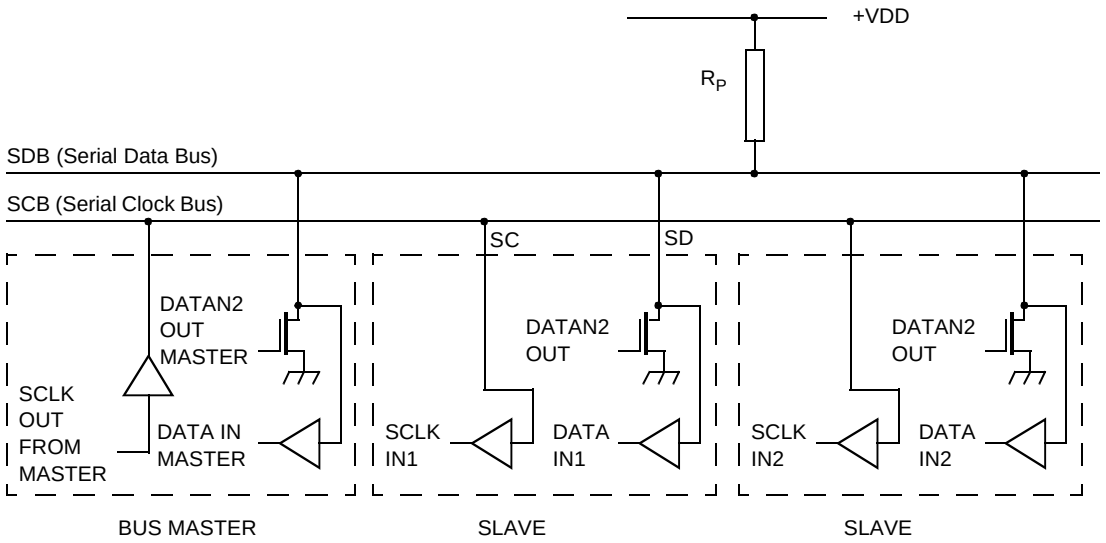


Figure 17: Connection of Devices to the Bus

Electrical Characteristics for Bus Devices

The electrical specifications of the bus devices' inputs and outputs and the characteristics of the bus lines connected to them are shown in **Figure 17**. A pull-up resistor (R_P) must be connected to a 5V +/- 10% supply. The CH7002 is a device with input levels related to VDD.

Maximum and minimum values of pull-up resistor (R_P)

The value of R_P depends on the following parameters:

- Supply voltage
- Bus capacitance
- Number of devices connected (input current + leakage current = I_{input})

The supply voltage limits the minimum value of resistor R_P due to the specified minimum sink current of 3mA at V_{OLmax} = 0.4 V for the output stages.

- $R_P >= (V_{DD} - 0.4) / 3$ (R_P in kΩ)

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_P due to the specified rise time. The equation for RP is shown below:

- $R_P <= 10^3/C$ (where R_P is in kΩ and C, the total capacitance, is in pF)

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 μA. Due to the desired noise margin of $0.2V_{DD}$ for the HIGH level, this input current limits the maximum value of R_P. The R_P limit depends on V_{DD} and is shown below:

- $R_P <= (100 \times V_{DD})/ I_{input}$ (where R_P is in kΩ and I_{input} is in μA)

Transfer Protocol

Both read and write cycles can be executed in "Alternating" and "Auto-increment" modes. Alternating mode expects a register address prior to each read or write from that location (i.e., transfers alternate between address and data). Auto-increment mode allows you to establish the initial register location, then automatically increments the register address after each subsequent data access (i.e., transfers will be address, data, data, data). A basic serial port transfer protocol is shown in **Figure 18** below.

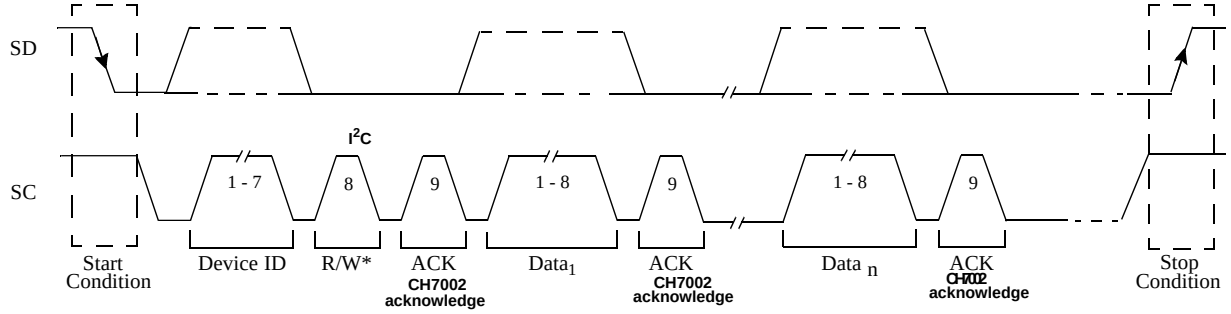


Figure 18: Serial Port Transfer Protocol

1. The transfer sequence is initiated when a high-to-low transition of SD occurs while SC is high, this is the "START" condition. Transitions of address and data bits can only occur while SC is low.
2. The transfer sequence is terminated when a low-to-high transition of SD occurs while SC is high, this is the "STOP" condition.
3. Upon receiving the first START condition, the CH7002 expects a ***Register Address Byte (RAB)*** from the master device. The format of the ***RAB*** byte is shown below (note that B[2:0] is determined by the state of the ADDR pin).

Device Address Byte (DAB)

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	1	ADDR*	ADDR	R/W

R/W **Read/Write Indicator**

"0": master device will write to the CH7002 at the register location specified by the address AR[3:0]

"1": master device will read from the CH7002 at the register location specified by the address AR[3:0.]. After the DAB is received, the CH7002 expects a Register Address Byte (RAB) from the master. The format of the RAB is shown below (note that B4, B5, and B7 are not used).

Register Address Byte (RAB)

B7	B6	B5	B4	B3	B2	B1	B0
1	AutoInc	X	X	AR[3]	AR[2]	AR[1]	AR[0]

AutoInc **Register Address Auto-Increment - to facilitate sequential r/w of registers.**

"1": Auto-Increment enabled (auto-increment mode).

Write: After writing data into a register, the Address Register will automatically be incremented by one.

Read: Before loading data from a register to the on-chip temporary register (getting ready to be serially read), the Address Register will automatically be incremented by one. The Address Register will not be changed for the first read after an RAB.

"0": Auto-Increment disabled (alternating mode).

Write: After writing data into a register, the Address Register will remain unchanged until a new RAB is written.

Read: Before loading data from a register to the on-chip temporary register (getting ready to be serially read), the Address Register will remain unchanged.

AR[3:0] **Specifies the Address of the Register to be Accessed.**

This register address is loaded into the Address Register of the CH7002. The R/W* access, which follows, is directed to the register specified by the content stored in the Address Register.

The following two sections describe the operation of the serial interface for the four combinations of R/W* = 0,1 and AutoInc = 0,1.

CH7002 Write Cycle Protocols (R/W = 0)

Data transfer with acknowledge is required. The acknowledge-related clock pulse is generated by the master-transmitter. The master-transmitter releases the SD line (HIGH) during the acknowledge clock pulse. The slave-receiver must pull down the SD line, during the acknowledge clock pulse, so that it remains stable LOW during the HIGH period of the clock pulse. The CH7002 always acknowledges for writes (see **Figure 19**). Note that the resultant state on SD is the wired-AND of data outputs from the transmitter and receiver.

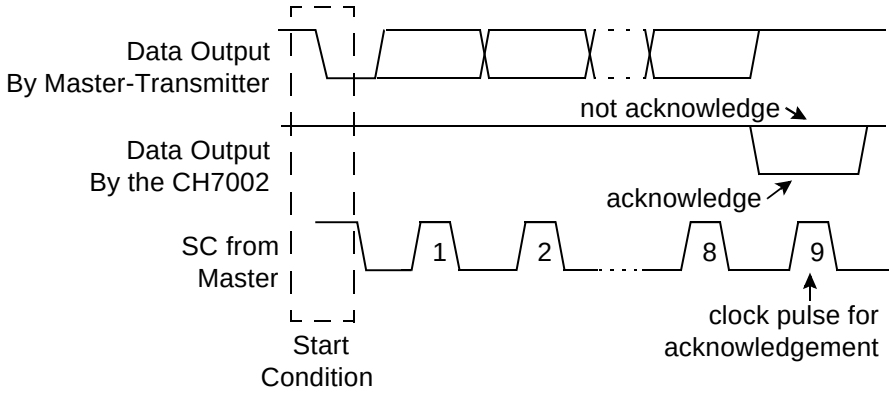


Figure 19: Acknowledge on the Bus

Figure 20 shows two consecutive alternating write cycles for AutoInc = 0 and R/W = 0. The byte of information, following the Register Address Byte (RAB), is the data to be written into the register specified by AR[3:0]. If AutoInc = 0, then another RAB is expected from the master device, followed by another data byte, and so on.

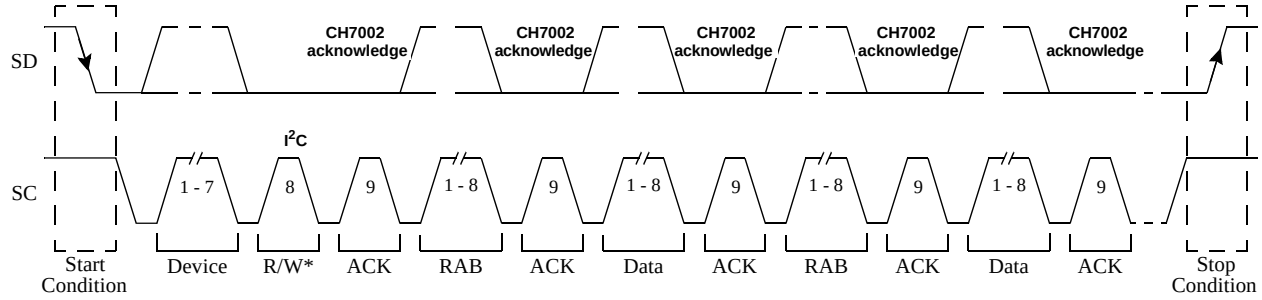


Figure 20: Alternate Write Mode

Note: * The acknowledge is from the CH7002 (slave).

If AutoInc = 1, then the register address pointer will be incremented automatically and subsequent data bytes will be written into successive registers without providing an RAB between each data byte. An Auto-increment write cycle is shown in **Figure 21**.

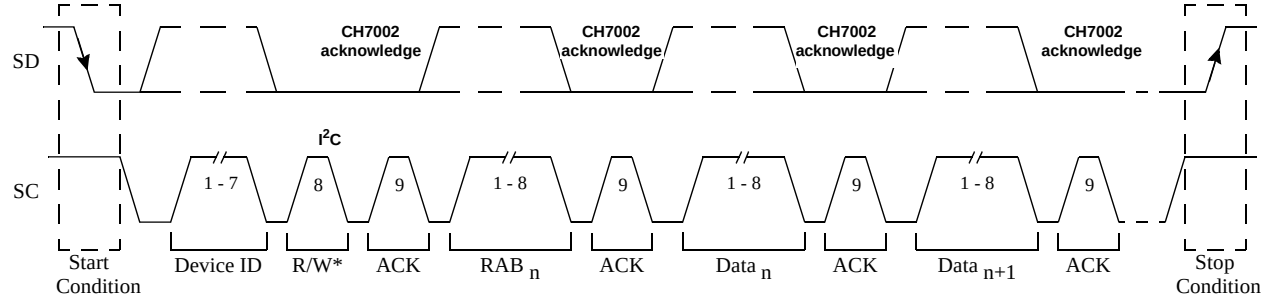


Figure 21: Auto-Increment Write Mode

Note: * The acknowledge is from the CH7002 (slave).

When the auto-increment mode is enabled (AutoInc is set to 1), the register address pointer continues to increment for each write cycle until AR[3:0] = 0Bh. (0Bh is the address of the Address Register.) The next byte of information represents a new auto-sequencing "Starting address," which is the address of the register to receive the next byte. The auto-sequencing then resumes based on this new "Starting address." The auto-increment sequence can be terminated anytime by either a "STOP" or "RESTART" condition. The write operation can be terminated with a "STOP" condition.

CH7002 Read Cycle Protocols (R/W* = 1)

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter CH7002 releases the data line to allow the master to generate the STOP condition or the RESTART condition.

To read the content of the registers, the master device starts by issuing a "START" condition (or a "RESTART" condition). The first byte of data, after the START condition, is a DAB with R/W = 1. The second byte is the RAB with AR[3:0], containing the address of the register that the master device intends to read, from in AR[3:0]. The master device should then issue a "RESTART" condition ("RESTART" = "START," without a previous "STOP" condition). The first byte of data, after this RESTART condition, is another DAB with R/W=0, indicating the master's intention to read data hereafter. The master then reads the next byte of data (the content of the register specified in the RAB). If AutoInc = 0, then another RESTART condition, followed by another DAB with R/W = 1 and RAB, is expected from the master device. The master device then issues another RESTART, followed by another DAB. Afterwards, the master may read another data byte, and so on. In summary, a RESTART condition,

followed by a DAB, must be produced by the master before each of the RAB, and before each of the data read events. Two consecutive alternating read cycles are shown in **Figure 22**.

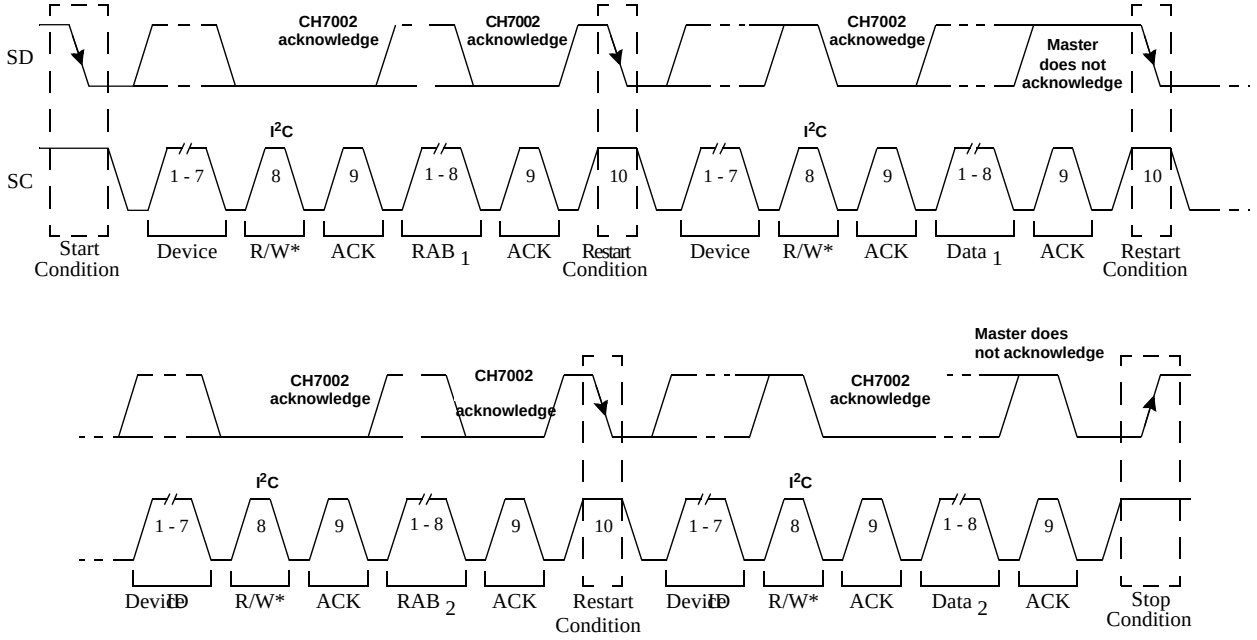


Figure 22: Alternate Read Mode

If AutoInc = 1, then the address register will be incremented automatically and subsequent data bytes can be read from successive registers, without providing a second RAB.

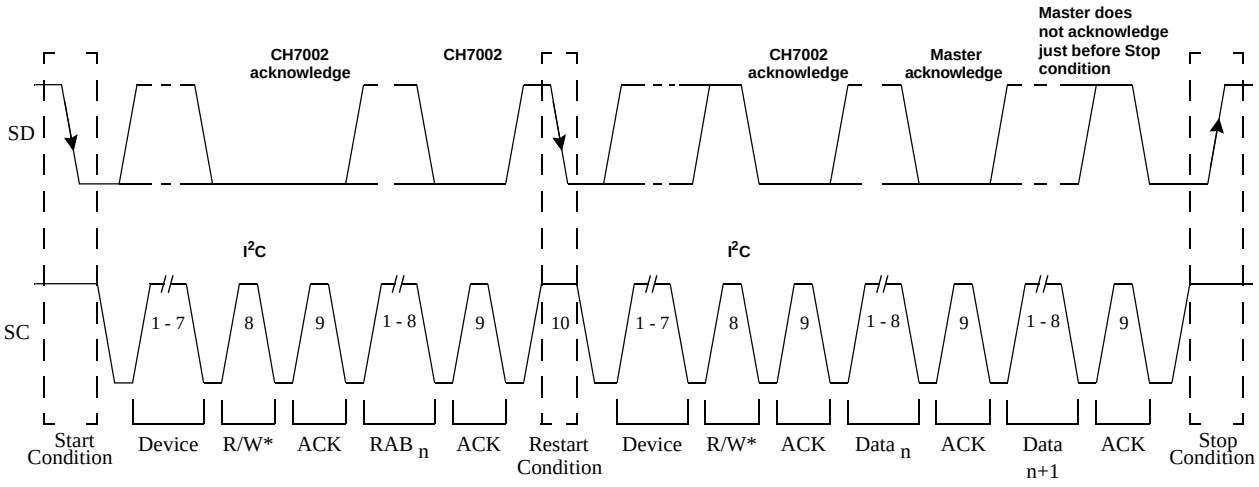


Figure 23: Auto-increment Read Mode

When the auto-increment mode is enabled (AutoInc is set to 1), the Address Register will continue incrementing for each read cycle. When the content of the Address Register reaches 0Bh, it will wrap around and start from 00h again. The auto increment sequence can be terminated by either a “STOP” or “RESTART” condition. The read operation can be terminated with a “STOP” condition. **Figure 23** shows an auto-increment read cycle terminated by a STOP or RESTART condition.

Registers and Programming

The CH7002 is a fully programmable device, providing for full functional control through the I^2C port, or partial functional control, through direct hardware pins. The CH7002 contains a total of 12 registers, which are listed in Table 5.

Table 5. Register Map

Register	Symbol	Address	Bits	Functional Summary
Display Mode	DMR	00H	3	Display mode selection
Flicker Filter	FFR	01H	2	Flicker filter mode selection
Y Filter	YFR	02H	3	Y (luma) filter bandwidth selection
Sampling Delay	SDR	03H	4	Sampling clock delay timing adjustment
Black Level	BLR	04H	7	Black level adjustment
Position Control	PCR	05H	4	Enables movement of displayed image on TV
Reserved		06H		Reserved for future use
Version ID	VIR	07H	3	Device version number
Miscellaneous Control	MCR	08H	8	Power management and other controls
Connection Detect	CDR	09H	4	Detection of TV presence
Test	TR	0AH	8	Reserved
Address	AR	0BH	4	Current register being addressed

Display Mode Register

Symbol: DMR
Address: 00H
Bits: 3

Bit:	7	6	5	4	3	2	1	0
Symbol:						DM2	DM1	DM0
Type:						R/W	R/W	R/W
Default:						0	1	0

This register provides programmable control of the CH7002 display mode, including input resolution, output TV format, and overscan/underscan scaling. The three-bit field, DM[2:0], selects the display mode to be used according to the following table of modes. Note that this programming of DM[2:0] is mutually exclusive to the pin-programming method (only one mode of programming may be used at any one time, based on the state of the PMODE pin).

DM2	DM1	DM0	Input Res	Output	Over/Under Scan
0	0	0	800x600	PAL	Underscan
0	0	1	640x480	PAL	Underscan
0	1	0	640x480	NTSC	Overscan
0	1	1	640x480	NTSC	Underscan
1	0	0	640x480	PAL	Overscan
1	0	1	800X600	PAL	Overscan
1	1	0	800x600	NTSC	Underscan
1	1	1	Reserved		

Register Descriptions (continued)

Flicker Filter Register

Symbol: FFR
Address: 01H
Bits: 2

Bit:	7	6	5	4	3	2	1	0
Symbol:							FF1	FF0
Type:							R/W	R/W
Default:							0	1

The flicker filter register provides for flicker filter mode selection, only when operating in Overscan modes (display modes 2 or 4). The low order bits of this register, FFR1 and FFR0, are logically "muxed" with the external pins MS1 and MS0 respectively. Flicker filter bits, FFR[1:0], form a two-bit value which corresponds to the flicker filter mode selection as follows:

FFR[1:0]	Mode	Comments
00	0:1:0	Flicker filtering is disabled
01	1:2:1	Moderate flicker filtering Default Mode
10	1:3:1	Low flicker filtering
11	1:1:1	High flicker filtering

Y (Luma) Filter Register

Symbol: YFR
Address: 02H
Bits: 3

Bit:	7	6	5	4	3	2	1	0
Symbol:						YPEAKD	YC-HI	YC-HI
Type:						R/W	R/W	R/W
Default:						0	0	0

This register enables the selection of alternative Luma filters for use with either composite or S-video outputs as well as the disabling of the Y-peaking circuit. In the default condition, the CH7002 is setup to use lower bandwidth filters with peaking enabled. Programming a "1" into each of these bit positions has the following effect:

Bit Position	Functional Description
CVBS-HI	Selects the high bandwidth filter for composite video outputs
YC-HI	Selects the high bandwidth filter for S-Video outputs and disables the Y-peaking circuit
YPEAKD	Disables the Y-peaking circuit

Sampling Delay Register

Symbol: SDR
Address: 03H
Bits: 4

Bit:	7	6	5	4	3	2	1	0
Symbol:					SD3	SD2	SD1	SD0
Type:					R/W	R/W	R/W	R/W
Default:					0	0	0	0

This register sets the delay timing, between the on-chip sampling clock and the sync signals, for the analog RGB inputs. The four least significant bits of this register provide a programmable delay value, in 15 programmable steps, with each step being 2.5 ns (nominal). As shown, the default value is 0 delay. Selecting a value of 4 creates a delay of 10 ns and a value of 8 places; the sampling delay is at the opposite phase of sampling the input signals.

Register Descriptions (continued)

Black Level Register

Symbol: BLR
Address: 04H
Bits: 7

Bit:	7	6	5	4	3	2	1	0
Symbol:		BL6	BL5	BL4	BL3	BL2	BL1	BL0
Type:		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default:		0	1	1	1	1	0	1

This register sets the black level, which is used as a relative baseline to reference the range of luminance values to be output. The first seven bits of this register, BL[6:0], provide a programmable black level value, which must be set between 51 and 80 (S-Video has limitation above 80), with the default of 61.

Position Control Register

Symbol: PCR
Address: 05H
Bits: 4

Bit:	7	6	5	4	3	2	1	0
Symbol:					LEFT	RIGHT	UP	DOWN
Type:					W	W	W	W
Default:					1	1	1	1

This register is used to shift the displayed TV image, in any orthogonal direction (left or right and up or down), to achieve a centered image on screen. Each of the first four bits of this register, DOWN, UP, LEFT, AND RIGHT, correspond to one of the basic directions of movement. As any of these bits are toggled (from 1 to 0 and back to 1), the displayed image shifts four pixels in that direction from its current location (e.g. toggling UP will move the TV image up by 4 input pixels). These four directional bits are bit-wise "ANDed," with the signals from the four corresponding input pins, so that position control can be effected at any time by using programming or toggle switches. Note that the image positioning will be reset (to initial condition) by toggling into certain display modes. When operating in modes 1 to 6, entering into mode 0 and returning will reset positioning. When operating in mode 0, entering into mode 1 and returning will also reset positioning. Resetting the position can be used to enable absolute position programming by starting from a known reference.

Version ID Register

Symbol: VIR
Address: 07H
Bits: 3

Bit:	7	6	5	4	3	2	1	0
Symbol:						VIR3	VIR1	VIR0
Type:						R	R	R
Default:						0	0	0

This read-only register contains a 3-bit value, indicating the identification number, assigned to this version of the CH7002. The default value shown is pre-programmed into this chip and is useful for checking the correct version of this chip before proceeding with its programming.

Register Descriptions (continued)

Miscellaneous Control Register

Symbol: MCR
Address: 08H
Bits: 8

Bit:	7	6	5	4	3	2	1	0
Symbol:	CEE	BUD	ECE	ECD2	SP0	Reserved	PD1	PD0
Type:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default:	0	0	0	0	0	0	1	1

This register provides control of a number of different and unrelated functions, segmented into the following: **Power Down** - The CH7002 provides programmable control of its operating states, including normal and three reduced power modes. Bits 0 and 1 of MCR setup these modes as follows:

PD[1:0]	Operating State	Functional Description
11	Normal (On):	All circuits and pins are active
10	S-Video Off:	Power is shut off to the unused DACs associated with Y and C outputs
01	Power Down:	Most pins and circuitry are disabled (except for the bandgap reference)
00	Composite Off:	Power is shut off to the unused DAC associated with CVBS output

Scratchpad Bits - One bit has been set aside as a scratchpad bit, with no on-chip control functions as a convenience for programming.

Control Bits - Several control bits are provided to enable/disable specific video control functions:

Symbol	Functional Description
ECE	External Clock Enable. Setting this bit enables the external clock input on the XCLK pin
BUD	Burst Update Clock Disable. Setting this bit disables the burst frequency counter updates
CEE	Contrast Enhancement Enable. Setting this bit enables a contrast enhancement circuit
ECD2	External clock divide by two enable. Setting this bit enables dividing the incoming pixel clock by two.

Connection Detect Register

Symbol: CDR
Address: 09H
Bits: 4

Bit:	7	6	5	4	3	2	1	0
Symbol:					Y	C	CVBS	SENSE
Type:					R	R	R	W
Default:					0	0	0	0

The Connection Detect Register provides a means to sense the connection of a TV to either S-Video or composite video outputs. The status bits, Y, C, and CVBS, correspond to both the DAC outputs for S-Video (Y and C outputs) and composite video (CVBS). However, the values contained in these status bits ARE NOT VALID until a sensing procedure is performed. Using this register requires a sequence of events to enable the sensing of outputs, then reading out the applicable status bits. The detection sequence works as follows:

1. Set the SENSE bit to a 1. This forces a constant current output onto the Y, C, and CVBS outputs. Note that during SENSE = 1, these 3 analog outputs are at steady state and no TV synchronization pulses are asserted.
2. Reset the SENSE bit to 0. This triggers a comparison between the voltage sensed on these analog outputs and the reference value expected (Vthreshold = 1.235V). If the measured voltage is below this threshold value, it is considered connected. If it is above this voltage, it is considered unconnected. During this step, each of the three status bits corresponding to individual analog outputs will be set if they are NOT CONNECTED.
3. Read the status bits. The status bits, Y, C, and CVBS (corresponding to S-Video Y and C outputs and composite video) now contain valid information which can be read to determine which outputs are connected to a TV. Again, a "0" indicates a valid connection, a "1" indicates an unconnected output.

Test Register

Symbol: TR
Address: 0AH
Bits: 8

Bit:	7	6	5	4	3	2	1	0
Symbol:	T7	T6	T5	T4	T3	T2	T1	T0
Type:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default:	0	0	0	0	0	0	0	0

The Test Register contains 8 bits which are reserved for implementing patterns and measurements for tests. Writing a logical one into each bit, in this register, places the chip in a specific test mode. These test modes are not documented for use herein, since they are used only for manufacturing test.

Address Register

Symbol: AR
Address: 0BH
Bits: 4

Bit:	7	6	5	4	3	2	1	0
Symbol:					AR3	AR2	AR1	AR0
Type:					R/W	R/W	R/W	R/W
Default:	0	0	0	0	X	X	X	X

The Address Register points to the register currently being accessed. Since the most significant four bits of all addresses are zero, this register contains only the four least significant bits, AR[3:0].

Application Information

Figure 24 on page 28 shows the basic power, input, control, and output connections of the CH7002 necessary to generate TV output from VGA analog (RGB) input signals. This connection shows the most simplified configuration, in which all control of the CH7002 modes and features are accomplished using the I^2C serial control port.

Basically, the CH7002 receives analog RGB as well as TTL-compatible horizontal and vertical sync signals from the VGA interface. In the configuration shown, the pixel clock is regenerated internally to the CH7002 using a "genlock" PLL and the HSYNC input as a reference frequency. A 14.31818 oscillator provides a frequency reference for color subcarrier generation.

Power Connections

The CH7002 has three separate sets of power connections to the external system. The AVDD connections supply power to the video ADCs and genlock PLL. The DVDD connections power the digital circuits, including memory, control, and signal processing functions. Finally, the VDD connection powers the S-Video and composite video DAC's and output circuits.

Normally, all power supply connections will be derived from a single board level supply bus. If the system includes other potentially noisy digital components, it is best to use a separate linear voltage regulator to power the CH7002.

As with all video frequency analog devices, careful attention to power supply distribution is essential to achieve optimum performance. A detailed discussion of recommended power supply distribution and decoupling methods is provided in the section entitled *PC Board Layout Guidelines*.

Analog Input Connections

The CH7002 processes the video signals received on the RGB input pins. The first step in processing is to convert the analog signals into corresponding digital values through the use of a triple, high-speed ADC. The analog input pins accommodate signals ranging between 0 and 750 mV; this range is compatible with the standard output of a VGA, properly terminated with a 37.5 ohms effective load.

The RC filter networks (see **Figure 24** on page 28) serve to bandlimit the input signals to avoid aliasing artifacts.

Typical Use Configuration

The VGA input configured for applications that do not require RGB buffering before the monitor is shown in **Figure 24**. In this configuration, 75 Ω input termination must be guaranteed by: termination by the monitor connection, discrete 75 Ω resistors on the PCB, or a dummy 75 Ω termination connector. The total RGB trace on the PCB must be kept as short as possible to avoid cable reflection problems.

Refer to crystal manufacturer specifications for proper load capacitances. The optional variable tuning capacitor is required only if the crystal oscillation frequency cannot be controlled to the required accuracy. The capacitance value for the tuning capacitor should be obtained from the crystal manufacturer.

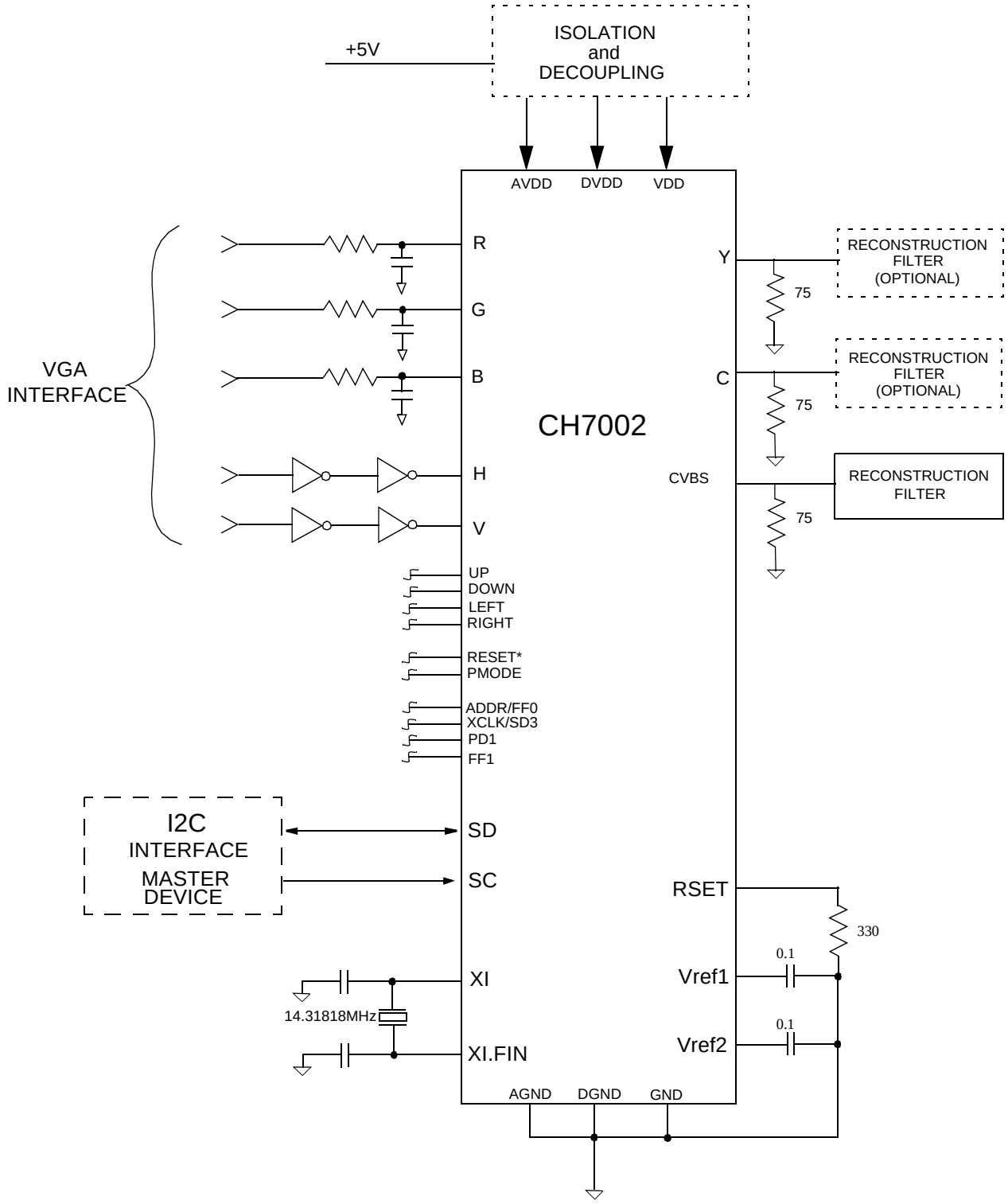


Figure 24: CH7002 Typical Connection Diagram

Analog Output Connections

The Y (luminance), C (chrominance), and CVBS (composite video, blanking and sync) outputs are direct current source outputs from the video DACs. An external shunt terminating resistor (nominally 75 ohms) is placed at the DAC outputs and serves to convert the current output to a voltage. Proper NTSC and PAL format output levels are achieved when the total effective termination is 37.5 ohms. External "reconstruction" filter networks are usually used to create a smooth and bandlimited output waveform. A reconstruction filter is recommended on the CVBS out to minimize image artifacts. The filters on the Y and C outputs often are not required and may unnecessarily limit signal bandwidth. **Figure 25** shows a typical reconstruction filter structure and component values.

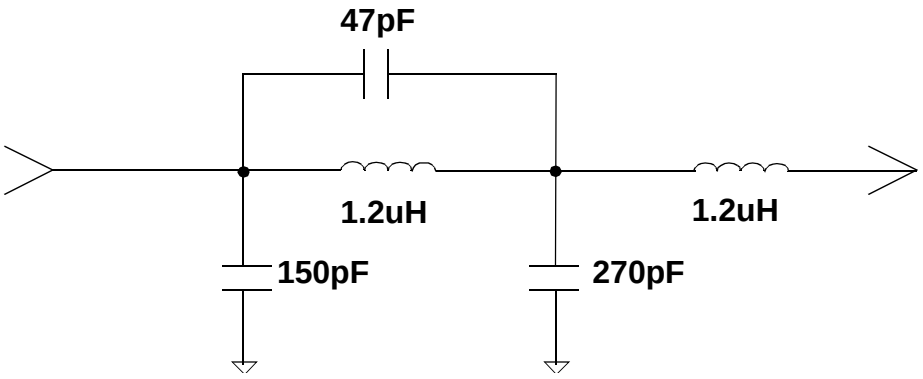


Figure 25: Typical Fourth-Order Reconstruction Filter

Control Interface

The operating modes of the CH7002 may be controlled either through dedicated digital input pins, or through the I^2C serial control interface. Selection of the control method is established by the PMODE pin; this pin should be strapped to either DVDD or GND, when the device is powered up, and should not be changed during operation.

When PMODE=1, the I^2C interface is enabled. Both of the SD/DM1 and SC/DM2 pins become the Serial Data and Serial Clock signals for the two-wire I^2C interface.

When PMODE= 0, the following pin functions are defined as:

- RESET*/DM0 becomes an input selecting CH7002 operating mode
- SD/DM1 becomes an input selecting CH7002 operating mode
- SC/DM2 becomes an input selecting CH7002 operating mode
- ADDR/FF0 becomes an input selecting CH7002 deflicker mode
- XCLK/SD3 becomes an input, selecting one of two analog input sample points

When pin control mode (PMODE=0) is selected, the function of the SC/DM2, SD/DM1, and RESET*/DM0 pins is identical to that of bits DM2, DM1, DM0 in configuration register DMR (Display Mode Register). The encoding of these inputs is restated in Table 6.

Table 6. Encoding Inputs Pin Control Mode

DM2	DM1	DM0	Input Resolution	Output Format	Scaling
0	0	0	800x600	PAL	Underscan
0	0	1	640X480	PAL	Underscan
0	1	0	640X480	NTSC	Overscan
0	1	1	640X480	NTSC	Underscan
1	0	0	640X480	PAL	Overscan
1	0	1	800X600	PAL	Overscan
1	1	0	800X600	NTSC	Underscan
1	1	1	Power Down	None	None

Position Control

The CH7002 defines four pins (UP, DOWN, LEFT, RIGHT) which provide a hardware-controlled positioning mechanism to adjust the horizontal and vertical position of the output image on the television screen. These inputs are rising edge-triggered, asynchronous, TTL-compatible inputs. They may be controlled from other logic devices such as I/O ports or microcontrollers, or may be connected to SPST switches directly. The inputs include an on-chip pull-up resistor so that only simple switch closures to ground are required. Care should be taken to avoid switch bounce. Also, simultaneous assertion of more than one of the four inputs should be avoided.

Crystal Oscillator

The CH7002 includes an oscillator circuit which allows an inexpensive 14.31818 MHz crystal to be connected directly. Alternatively, an externally generated 14.31818 MHz clock source may be supplied to the CH7002. If an external source is used, it should have TTL level specifications. The clock should be connected to the XO/FIN pin (pin 18), and the XI pin (pin 17) should be tied to ground. An external source should also exhibit +/- 50 ppm or better frequent accuracy, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

- Crystal is specified as 14.31818 MHz, +/- 50 ppm in parallel resonance
- Crystal is operated with a load capacitance equal to its specified value
- External load capacitors have their ground connection very close to the CH7002
- To allow tunability, a variable cap may be used from XI to ground

Note that the XI and XO/FIN pin each have approximately 15-10 pF of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI and XO/FIN pins, the following calculation should be used:

Cext = (2 * Cload) - Cint

where external load capacitance shall include routing capacitance on the PCB:

Cext = External load capacitance required on XI and XO/FIN nodes

Cload = Crystal load capacitance specified by crystal manufacturer

Cint = Capacitance internal to CH7002 (approximately 15-10 pF on each of XI and XO/FIN pins)

PC Board Layout Guidelines

The CH7002 is a high performance, mixed-signal IC containing precision analog and digital circuits. This section provides general guidelines for CH7002 PCB layout. Information on the ground plane, power planes, power supply decoupling, and layout for critical analog/digital signals and circuitry are included. The following design guidelines are intended to optimize the layout for minimum signal coupling. These are only recommendations. The user is urged to implement the configurations and evaluate the performance of the entire system before bringing the design to production.

Two-Layer vs. Four-Layer Designs

The CH7002 can be successfully used in either double-sided PCB applications, or PCB designs using four (or more) layers of interconnect. Using at least four layers will usually simplify the design task, and may also lower radiated emissions. In either case, the use of ground and power planes are necessary to achieve full performance. Ground and power planes should fill all available PCB areas not used for routing signals.

In the case of 4-layer designs, the recommended layer utilization is as follows:

- Layer 1 (top): Analog interconnections
- Layer 2: Ground plane
- Layer 3: Power supply planes
- Layer 4: Digital interconnections

If a 2-layer design is used, the layer utilization should be:

- Layer 1: Analog interconnects, area-filled power supply planes
- Layer 2: Digital interconnects, area-filled ground plane

Placement Considerations

The CH7002 device should be placed in close proximity with other analog components it connects to, or shares power connections. Conversely, the device should be located as far as possible from noise-producing digital components such as microprocessors, DRAM arrays, system clock generators, etc.

Power Distribution and Decoupling

As previously described, the CH7002 has three separate sets of power connections to the external system. Normally, all power supply connections will be derived from a single board level supply bus. If the system includes other potentially noisy digital components, it is best to use a separate linear voltage regulator to power the CH7002.

The three power buses should be isolated from each other through the use of ferrite beads. Surface mount beads, having a nominal impedance of 55-60 ohms at 100MHz, are usually effective.

It is critically important that all power supply connections be effectively decoupled. Each power pin should be decoupled to its "associated" ground pin (see Table 7), with a high-quality ceramic surface mount capacitor. These capacitors should be placed as close as possible to the device pins; the preferred value is 0.1 uF. In the case of especially noisy environments, greater decoupling effectiveness can be achieved by adding a 0.01 uF ceramic cap in parallel with each 0.1 uF cap. The 0.01 uF cap provides greater bypassing of very high frequency noise. Each CH7002 ground pin should be directly connected to its respective decoupling capacitor lead; then, both the pin and the lead should be connected to the ground plane. If possible, a physical connecting trace between the CH7002 ground pin and the capacitor lead should be present on the connecting layer, rather than relying on the ground plane alone for the connections. All ground traces should be short and wide, with multiple ground vias to minimize parasitic inductance. A recommended power supply isolation and decoupling strategy is detailed in **Figure 27** on page 33.

Table 7. Power and Ground Pin Decoupling

Power Pin	Pin Number	Associated Ground Pin
DVDD1	8	10
DVDD2	14	16
DVDD3	33	31
VDD1	25	21
AVDD1	44	2
AVDD2	7	6
AVDD3	37	39
AVDD4	40	42

Power Supply Sequencing

It is important to ensure that the three separate power supply rails of theCH7002 (VDD, AVDD, and DVDD) are applied simultaneously during the power-up process. Failure to do so may, in rare instances, put the CH7002 into a non-functional "latchup" condition, which can possibly destroy the device.When the power rails are derived from a single 5 volt source as shown in Figure 27, sequencing is not an issue and the latchup problem will not occur. In some designs, however, the analog (AVDD, VDD) and digital (DVDD) supplies may be derived from separate sources such as the separate outputs of a multi-output switching power supply. In this case, significant delays may be created between application of the analog and digital voltages, creating the potential latchup condition.

Whenever the possibility of power sequencing delays exist, the design should include back-to-back connected diodes coupling the analog and digital supply rails, as shown in Figure 27.

Using this arrangement, the first supply to come up will "pull" the other supply rail along with it, eliminating the latchup potential. Use of rectifier-type diodes with at least 400mA forward current ratings is suggested. It is suggested that the diodes be connected on the power-supply side of any ferrite beads or other isolation networks

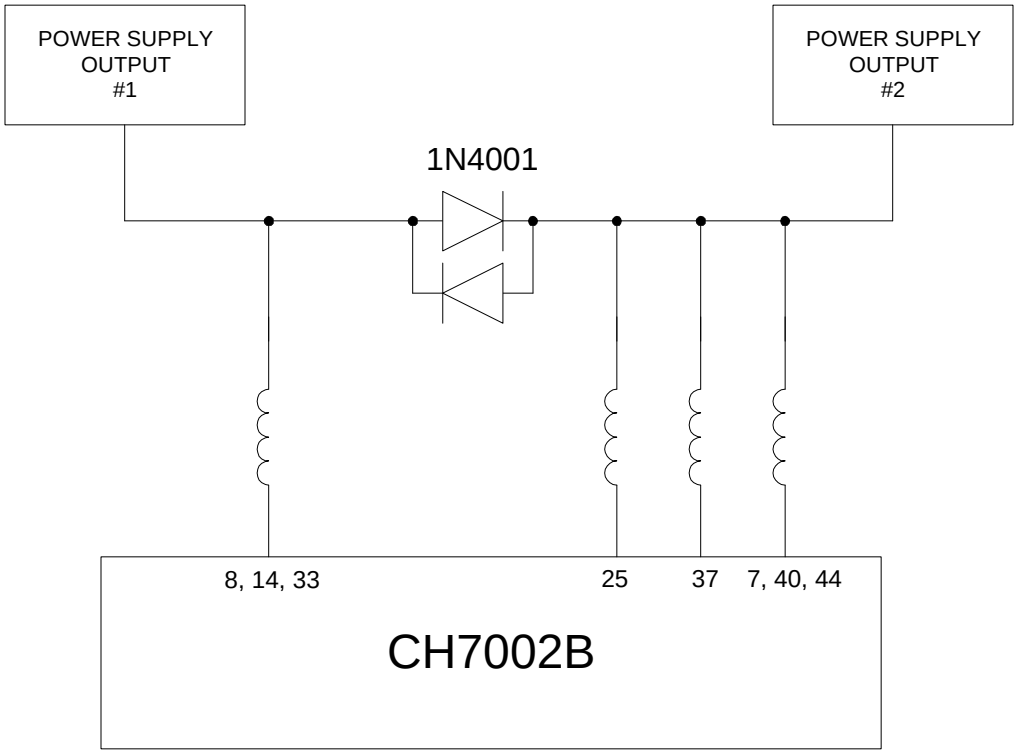


Figure 26: Power Sequencing

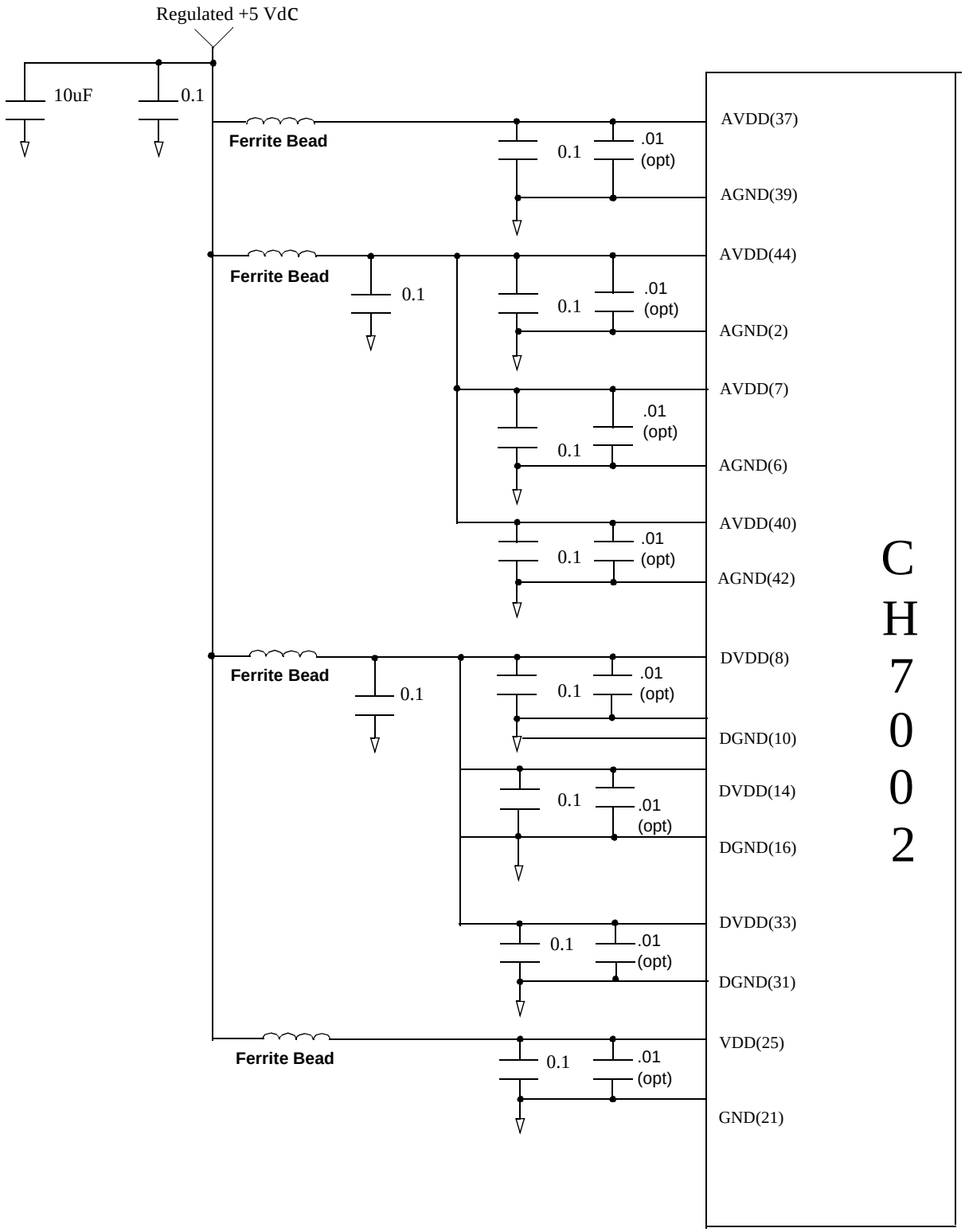


Figure 27: Power Supply Isolation Decoupling Configuration

Optional Controls and Circuits

Full Scale Input Range Adjustment

The full-scale input range of the CH7002 may be modified from its nominal value of 750 mV. This is accomplished by forcing a DC voltage into the VREF1 pin, thus overriding the internally-generated reference voltage. The simple circuit shown below allows adjustment of the VREF1 voltage, over approximately a 1.0 to 2.5 volt range.

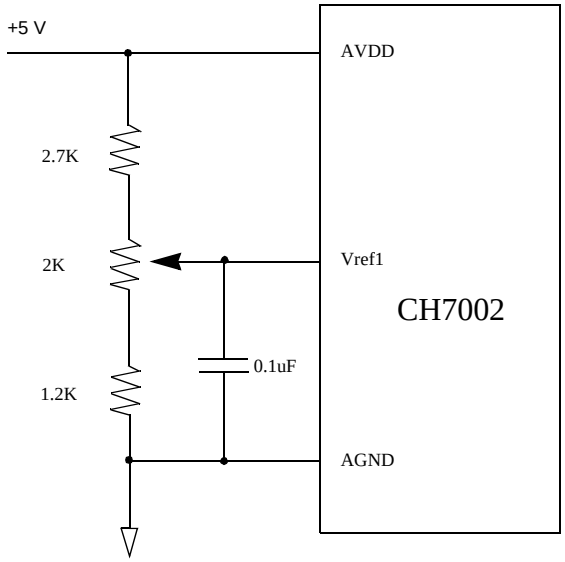


Figure 28: Full-Scale Input Range Adjustment

Electrical Specifications

Table 8. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	VDD relative to GND	- 0.5		7.0	V
	Input voltage of all digital pins	GND - 0.5		Vdd + 0.5	V
TSC	Analog output short circuit duration		Indefinite		Sec
TAMB	Ambient operating temperature	- 55		70	° C
TSTOR	Storage temperature	- 65		150	° C
TJ	Junction temperature			150	° C
TVPS	Vapor phase soldering (one minute)			220	° C
PMAX	Maximum power dissipation			1.9	W

Notes:

1 Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions section of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2 The device is fabricated using high-performance CMOS technology. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5V can induce destructive latchup.

3 The temperature assumes a still environment with no active cooling.

Electrical Specifications (Continued)

Table 9. Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
VDD	DAC power supply voltage	4.75	5.00	5.25	V
AVDD	Analog supply voltage		5.00		
DVDD	Digital supply voltage		5.00		
T_A	Ambient operating temperature[3]	0	25	70	°C
R_L	Output load to DAC outputs		37.5		Ohms
VREF1	ADC voltage reference input/output	1.14	1.235	1.26	V
VREF2	Internal voltage reference		2.5		V

Table 10. Electrical Characteristics (Operating Conditions: $T_A = 0^oC - 70^oC$, $V_{DD} = 5V \pm 5\%$)

Symbol	Description	Min	Typ	Max	Unit
	Video D/A resolution	8	8	8	Bits
	Full scale output current		33.89		mA
	Video level error using external reference using internal reference			 5 10	 % %
IREF1	VREF1 input current (VREF1 = 1.235V)		10		µA
	Total Current Consumption		345		mA

Note: As applied to Tables 6, 7, and 8, Recommended Operating Conditions are used as test conditions unless otherwise specified. External voltage reference used with RSET = 324Ω, VREF1 = 1.235V.

Table 11. Digital Inputs / Outputs

Symbol	Description	Test Condition @ $T_A = 25^oC$	Min	Typ	Max	Unit
V_{OH}	Output high voltage	Ioh = - 400 mA	2.4			V
V_{OL}	Output low voltage	Iol = 3.2 mA			0.4	V
V_{IH}	Input high voltage		2.0		Vdd + 0.5	V
V_{IL}	Input low voltage		GND - 0.5		0.8	V
I_{PU}	Input internal pull-up current		5		25	mA
I_{LK}	Input leakage current		-10		10	mA
CD_{IN}	Input capacitance	f = 1 MHz, Vin = 2.4V		7		pF
CD_{OUT}	Output capacitance			10		pF

Table 12. Timing

Symbol	Description	Min	Typ	Max	Unit
t_1	Sync to external clock setup time		2		nS
t_2	Sync to external clock hold time		2		nS

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH7002D-V	PLCC	44	5V

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